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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,042	06/24/2003	Erh-Kun Lai	9265-US-PA	1041

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
KENNEDY, JENNIFER M	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,042	LAI ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *13-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/24/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Applicant's election of claims 1-12 in the reply filed on April 29, 2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 13-24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Objections

Claim 8 is objected to because of the following informalities: line 3 requires that conductive layers to be a titanium nitride layer. The examiner notes that the specification has nothing directed to a titanium nitride layer. The examiner believes this is a typographical error and was intended to be titanium silicide. The examiner points applicants' attention to claim 12, which recites titanium silicide. Examination will be made accordingly. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In re claim 1, Applicants require a first stack and a second stack crossing over each other the first stack and the second stack requiring a pair of conductive layers in addition to other limitations. The examiner notes throughout the specification and drawings that the top conductive layer of the first stack is the bottom conductive layer of the second stack (see for example Figure 2A and 2B, 25 is the top conductive layer of the first stack and the bottom conductive layer of the second stack). However, as claimed a pair of first conductive layers and a pair of second conductive layer require four conductive layers, while Applicants' invention only requires 3 conductive layers for the two stacks (see for example Figure 2A and 2B, where the first pair of conductive layers are 23 and 25, and the second pair of conductive layers are 25 and 35).

Further the examiner notes that since layer 25 is used for both the first and second stack, 25 can not possibly cross over itself. Therefore it is noted that only a portion of the two stacks cross over each other.

Claim 9, also has a similar problem in that the last C of the C/A/N/P/C line is the first C of the C/A/P/N/C line. It is also impossible for the same layer to cross over itself as claimed.

Claims 2-8 and 10-11 are rejected for being dependent on rejected claims 1 and 9.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-10, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson et al. (U.S. Patent No. 6,351,406).

In re claim 1 with respect to claims 2 and 3, Johnson et al. disclose a three-dimensional memory structure, comprising a first stack circuit (conductor 1 and associated stack), having:

a pair of first conductive layers (46, 48);

a first first-type polysilicon layer (41) between the first conductive layers;

a first second-type polysilicon layer (40) between the first first-type polysilicon layer and one of the first conductive layers (46); and

a first anti-fuse (42) between the first first-type polysilicon layer and the other one of the first conductive layers (48); and

a second stack circuit crossing (conductor 2 through conductor 4 and the associated stack is being considered the second stack circuit) over the first stacked circuit, having:

a pair of second conductive layers (48 of conductor 2 and 4);

a second second-type polysilicon layer (40 of conductor 2) between the second conductive layers ;

a second first-type polysilicon layer (43 of conductor 2) between the second second-type polysilicon layer and one of the second conductive layers (48 of conductor 2); and

a second anti-fuse between (42 of conductor 2) the second second-type polysilicon layer and the other one of the second conductive layers (48 of conductor 4, see column 11, line 40 through column 12, line 41, Figures 5 and 6a).

The examiner notes that in Johnson et al. conductor 2 and 4 cross over conductor 1.

In re claim 2, Johnson et al. disclose the memory structure of claim 1, wherein the first first-type polysilicon layer (41) and the second first-type polysilicon layer (43) include an n-type polysilicon layer.

In re claim 3, Johnson et al. disclose the memory structure of claim 2, wherein the first second- type polysilicon layer (40 of conductor 1) and the second second-type polysilicon layer (40 of conductor 4) include a p-type polysilicon layer.

In re claim 1, with respect to claims 4 and 5, Johnson et al. disclose a three-dimensional memory structure, comprising a first stack circuit (conductor 1 and 3 and associated stack), having:

a pair of first conductive layers (48 of conductor 1 and 3);

a first first-type polysilicon layer (40 of conductor 1) between the first conductive layers;

a first second-type polysilicon layer (41 of conductor 1) between the first first-type polysilicon layer and one of the first conductive layers (48 of conductor 1); and

a first anti-fuse (42 of conductor 1) between the first first-type polysilicon layer (40 of conductor 1) and the other one of the first conductive layers (48 of conductor 3); and

a second stack circuit (conductor 4 and associated stack) crossing over the first stacked circuit, having:

a pair of second conductive layers (46, 48 of conductor 4);

a second second-type polysilicon (41 of conductor 4) layer between the second conductive layers;

a second first-type polysilicon layer (40 of conductor 4) between the second second-type polysilicon layer and one of the second conductive layers (46 of conductor 4); and

a second anti-fuse (42 of conductor 4) between the second second-type polysilicon layer (41 of conductor 4) and the other one of the second conductive layers (48).

The examiner notes that in Johnson et al. conductor 4 crosses over conductor 1 and 3

In re claim 4, Johnson et al. disclose the memory structure of claim 1, wherein the first first-type polysilicon layer (40 of conductor 1) and the second first-type polysilicon layer (40 of conductor 4) include a p-type polysilicon layer.

In re claim 5, Johnson et al. disclose the memory structure of claim 4, wherein the first second- type polysilicon layer (41 of conductor 1) and the second second-type polysilicon layer (41 of conductor 4) include an n-type polysilicon layer.

In re claim 6, Johnson et al. disclose the memory structure of claim 1, wherein the first anti-fuse and the second anti-fuse include an oxide layer (see Figure 6a and column 12, lines 1-12).

In re claim 8, Johnson et al. disclose the memory structure of claim 1, wherein the first conductive layers and the second conductive layers include a titanium silicide layer (see column 12, lines 30-41).

In re claim 9, Johnson et al. disclose a three-dimensional memory structure, comprising:

a C/A/N/P/C line, wherein N is an n-type polysilicon layer, C is a conductive layer, A is an anti-fuse and P is a p-type polysilicon layer (see Figures 5 and 6a and column 11 line 40 through column 12 line 41); and

a C/A/P/N/C line crossing over the C/A/N/P/C line (see Figures 5 and 6a and column 11 line 40 through column 12 line 41).

The examiner notes that as broadly as can be interpreted claim 9 does not require an sequential order of layers.

In re claim 10, Johnson et al. disclose the memory structure of claim 9, wherein the anti-fuse structure includes an oxide layer (see Figure 6a and column 12, lines 1-12).

In re claim 12, Johnson et al. disclose the memory structure of claim 9, wherein the conductive layer includes a titanium silicide layer (see column 12, lines 30-41).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (U.S. Patent No. 6,351,406).

In re claim 7 and 11, Johnson et al. discloses the device as claimed and rejected above, but does not disclose wherein the first conductive layers and the second conductive layers include a tungsten silicide layer. Johnson does disclose that refractory metals such as tungsten may be used for the conductors and that metal silicides are also desirable for the conductors (see column 14, lines 59-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive layer of tungsten silicide since as Johnson et al. teaches tungsten may be used and metal silicides are more preferable because they are compatible with the higher temperatures process required for the activation of the dopants and since it has been held to be within the general skill of the worker in the art

to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

In re claim 8, the examiner has provided a rejection, if indeed the Applicants intended on reciting a titanium nitride layer. Johnson et al. discloses the device as claimed and rejected above, but does not disclose the use of titanium nitride. Johnson et al. discloses that titanium nitride is useful as barrier layer surrounding the metal layers and thus part of the conductive layers (see column 16, lines 21-29) it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive layers including titanium nitride in order to prevent diffusion of the electrode material into the device layer during processing.

If indeed the Applicants intended on reciting a titanium nitride layer the examiner suggest the Applicants' amend the specification to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812